JDEP 284H

Foundations of Computer Systems

Cache Memories

Dr. Steve Goddard goddard@cse.unl.edu

http://cse.unl.edu/~goddard/Courses/JDEP284

Giving credit where credit is due

- Most of slides for this lecture are based on slides created by Drs. Bryant and O'Hallaron, Carnegie Mellon University.
- I have modified them and added new slides.

Topics

- ■Generic cache memory organization
- ■Direct mapped caches
- ■Set associative caches
- ■Impact of caches on performance

Cache Memories

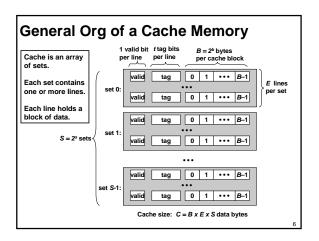
Cache memories are small, fast SRAM-based memories managed automatically in hardware.

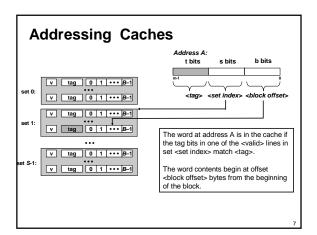
Hold frequently accessed blocks of main memory

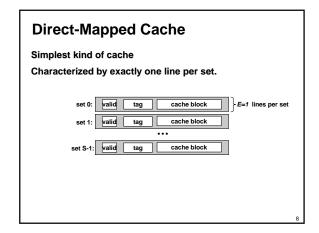
CPU looks first for data in L1, then in L2, then in main memory.

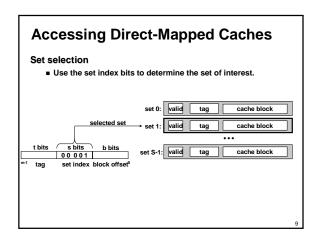
Typical bus structure:

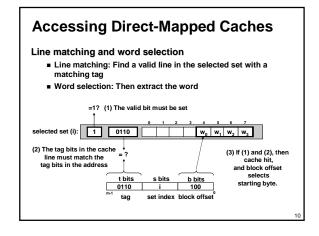
Inserting an L1 Cache Between the CPU and Main Memory The tiny, very fast CPU **register file** has room for four 4-byte words. The transfer unit between the CPU register file and the cache is a 4-byte block. line 0 The small fast L1 cache has room for two 4-word blocks. The transfer unit between the cache and main memory is a 4-word block (16 bytes). block 10 abcd The big slow main memory has room for many 4-word pqrs blocks. wxyz

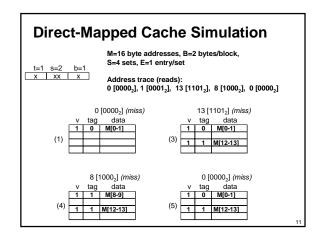


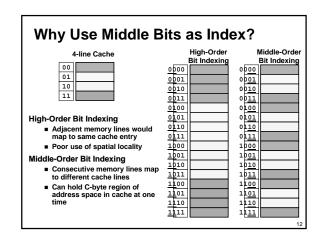


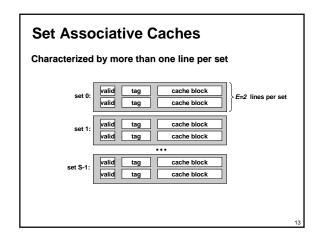


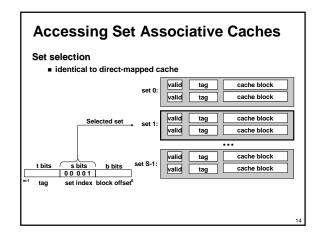


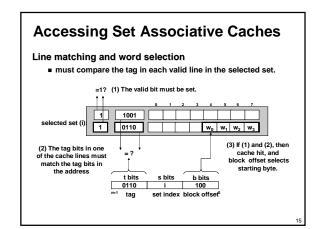


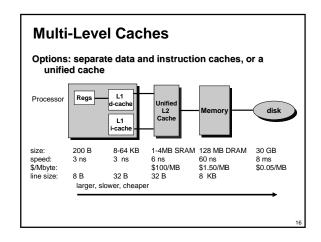


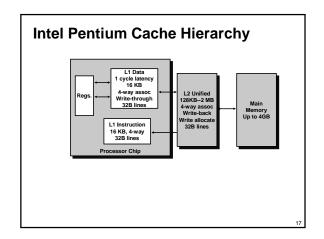












Cache Performance Metrics Miss Rate Fraction of memory references not found in cache (misses/references) Typical numbers: 3-10% for L1 can be quite small (e.g., < 1%) for L2, depending on size, etc. Hit Time Time to deliver a line in the cache to the processor (includes time to determine whether the line is in the cache) Typical numbers: 1 clock cycle for L1 3-8 clock cycles for L2 Miss Penalty Additional time required because of a miss Typically 25-100 cycles for main memory

Writing Cache Friendly Code

Repeated references to variables are good (temporal iocality)

Stride-1 reference patterns are good (spatial locality) **Examples:**

■ cold cache, 4-byte words, 4-word cache blocks

```
int sumarrayrows(int a[M][N])
       for (i = 0; i < M; i++)
  for (j = 0; j < N; j++)
    sum += a[i][j];
return sum;</pre>
```

```
int sumarraycols(int a[M][N])
        int i, j, sum = 0;
        for (j = 0; j < N; j++)
  for (i = 0; i < M; i++)
      sum += a[i][j];
return sum;</pre>
```

Miss rate = 1/4 = 25%

Miss rate = 100%

The Memory Mountain

Read throughput (read bandwidth)

■ Number of bytes read from memory per second (MB/s)

Memory mountain

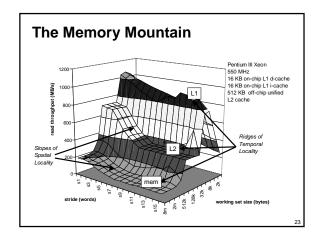
- Measured read throughput as a function of spatial and temporal locality.
- Compact way to characterize memory system performance.

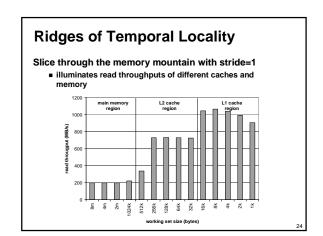
Memory Mountain Test Function

```
/* The test function */
void test(int elems, int stride) {
  int i, result = 0;
  volatile int sink;
     for (i = 0; i < elems; i += stride)
    result += data[i];
sink = result; /* So compiler doesn't optimize away the loop */</pre>
/* Run test(elems, stride) and return read throughput (MB/s) */double run(int size, int stride, double Mhz)
     double cycles;
int elems = size / sizeof(int);
```

Memory Mountain Main Routine

```
/* mountain.c - Generate the memory mountain. */
#define MINBYTES (1 << 10) /* Working set size ranges from 1 KB */
#define MAXBYTES (1 << 23) /* ... up to 8 MB */
#define MAXSTRIDE 16 /* Strides range from 1 to 16 */
#define MAXELEMS MAXBYTES/sizeof(int)
int data[MAXELEMS];
                                                                             /* The array we'll be traversing */
int main()
         int size;
int stride;
double Mhz;
                                                       /* Working set size (in bytes) */
/* Stride (in array elements) */
/* Clock frequency */
        init_data(data, MAXELEMS); /* Initialize each element in data to 1 */
Mhr = mhr(0); /* Estimate the clock frequency */
for (size = MAXEYTES; size >= MINEYTES; size >>= 1) {
    for (stride = 1; stride <= MAXSTRIDE; stride++)
        printf(*%.1f\t*, run(size, stride, Mhz));
    printf(*\n*);
}</pre>
            exit(0):
```

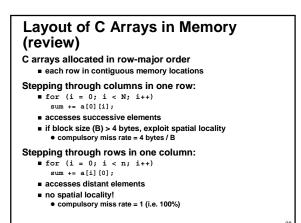


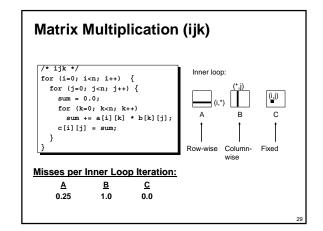


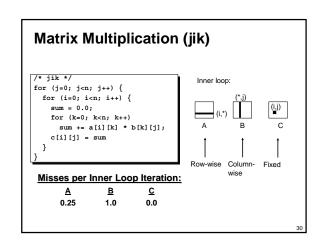
A Slope of Spatial Locality Slice through memory mountain with size=256KB shows cache block size. strice (words)

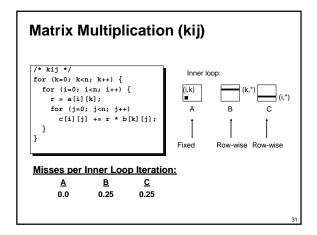
Matrix Multiplication Example Major Cache Effects to Consider ■ Total cache size • Exploit temporal locality and keep the working set small (e.g., by using /* ijk */ Variable sum for (i=0; i<n; i++) { held in register ■ Block size for (j=0; j<n; j++) { sum = 0.0; Exploit spatial locality for (k=0; k<n; k++) sum += a[i][k] * b[k][j]; Description: c[i][j] = sum; ■ Multiply N x N matrices ■ O(N^3) total operations ■ Accesses N values summed per destination » but may be able to hold in register

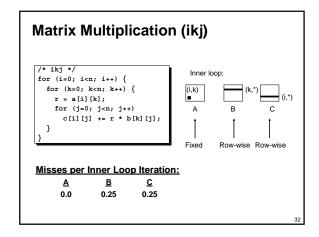
Miss Rate Analysis for Matrix Multiply Assume: Line size = 32B (big enough for 4 64-bit words) Matrix dimension (N) is very large Approximate 1/N as 0.0 Cache is not even big enough to hold multiple rows Analysis Method: Look at access pattern of inner loop

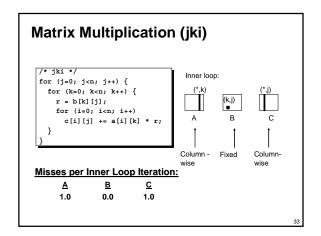


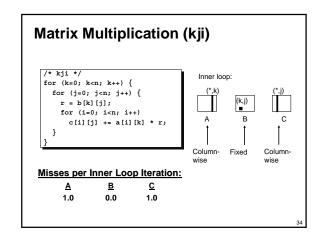


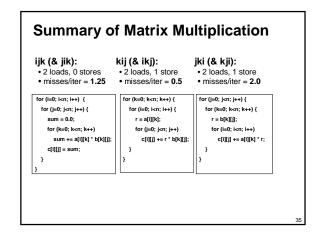


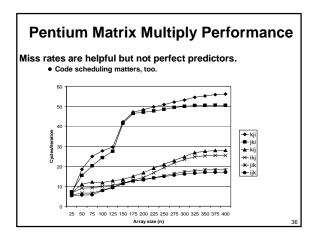












Improving Temporal Locality by **Blocking**

Example: Blocked matrix multiplication

- "block" (in this context) does not mean "cache block".
- Instead, it means a sub-block within the matrix.
- Example: N = 8; sub-block size = 4

$$\begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \quad X \quad \begin{bmatrix} B_{11} & B_{12} \\ B_{21} & B_{22} \end{bmatrix} \quad = \quad \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix}$$

 $\underline{\text{Key idea:}}$ Sub-blocks (i.e., $\boldsymbol{A}_{xy}\!)$ can be treated just like scalars.

$$\begin{split} C_{11} &= A_{11}B_{11} + A_{12}B_{21} & C_{12} &= A_{11}B_{12} + A_{12}B_{22} \\ C_{21} &= A_{21}B_{11} + A_{22}B_{21} & C_{22} &= A_{21}B_{12} + A_{22}B_{22} \end{split}$$

```
Blocked Matrix Multiply (bijk)
        for (jj=0; jj<n; jj+=bsize) {
  for (i=0; i<n; i++)</pre>
              for (j=jj; j < min(jj+bsize,n); j++)
c[i][j] = 0.0;
          c(i)[j] = 0.0;
for (kk=0; kk-n; kk+=bsize) {
  for (i=0; i<n; i++) {
    for (j=jj; j < min(jj+bsize,n); j++) {
    sum = 0.0
    for (k=kk; k < min(kk+bsize,n); k++) {</pre>
                         sum += a[i][k] * b[k][j];
                     c[i][j] += sum;
              }
```

Blocked Matrix Multiply Analysis

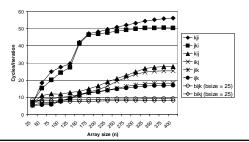
- Innermost loop pair multiplies a 1 X bsize sliver of A by a bsize X bsize block of B and accumulates into 1 X bsize sliver of C

```
■ Loop over i steps through n row slivers of A & C, using same B
    sum = 0.0
for (k=kk; k < min(kk+bsize,n); k++) {
  sum += a[i][k] * b[k][j];</pre>
              c[i][j] += sum;
Loop Pair
                                                         Update successive
                      row sliver accessed
                                                          elements of sliver
                     hsize times
                                       block reused \boldsymbol{n}
                                       times in succession
```

Pentium Blocked Matrix Multiply Performance

Blocking (bijk and bikj) improves performance by a factor of two over unblocked versions (ijk and jik)

■ relatively insensitive to array size.



Concluding Observations

Programmer can optimize for cache performance

- How data structures are organized
- How data are accessed
 - Nested loop structure
 - Blocking is a general technique

All systems favor "cache friendly code"

- Getting absolute optimum performance is very platform specific
 - Cache sizes, line sizes, associativities, etc.
- Can get most of the advantage with generic code
 - Keep working set reasonably small (temporal locality)
 - Use small strides (spatial locality)